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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,474	10/17/2001	David P. Tester	01-587 1496.00157	6044

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LSI LOGIC CORPORATION  
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 MILPITAS, CA 95035

EXAMINER
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SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/981,474

Applicant(s)

TESTER, DAVID P.

Examiner

Suresh K Suryawanshi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 11-20 is/are rejected.
- 7) ☒ Claim(s) 10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 October 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Claims 1-20 are presented for examination.

#### ***Drawings***

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "104" at page 9, line 2, 6, 7, 10. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 7-8, 11, 17-18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Melava et al (US Patent no 6,583,674 B2).

6. As per claim 1, Melava et al teach a prescaler comprising:

a first circuit configured to present a plurality of control signals in response to a first clock signal having a first frequency [Fig. 4; col. 4, lines 40-46; circuit 402];

a multiplexer configured to multiplex a plurality of data signals in response to said control signals to preset a second clock signal having a second frequency that is a non-integer fraction of said first frequency [Fig. 4; col. 4, line 61 -- col. 5, line 3; a multiplexer 403; col. 3, lines 42-44]; and

a second circuit configured to present said data signals in response to said second clock signal [Fig. 4; col. 5, lines 4-8; circuit 404].

7. As per claim 11, Melava et al teach a method of dividing a first clock signal having a first frequency, the method comprising the steps of:

generating a plurality of control signals in response to said first clock signal [Fig. 4; col. 4, lines 40-46; circuit 402 generates a plurality of control signals in response to an input signal];

multiplexing a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency [Fig. 4; col. 4, line 61 -- col. 5, line 3; a multiplexer 403; col. 3, lines 42-44]; and

generating said data signals in response to said second clock signal [Fig. 4; col. 5, lines 4-8; circuit 404].

8. As per claim 20, Melava et al teach a prescaler comprising:

means for generating a plurality of control signals in response to said first clock signal [Fig. 4; col. 4, lines 40-46; circuit 402 generates a plurality of control signals in response to an input signal];

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means for multiplexing a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency [Fig. 4; col. 4, line 61 -- col. 5, line 3; a multiplexer 403; col. 3, lines 42-44]; and

means for generating said data signals in response to said second clock signal [Fig. 4; col. 5, lines 4-8; circuit 404].

9. As per claims 7-8 and 17-18, having at least one or two of said control signals in an active state at a time will be inherent to the system as the multiplexing depends on it [Fig. 4; col. 4, line 61 -- col. 5, line 3; a multiplexer 403].

### ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 2-6, 9, 12-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melava et al (US Patent no 6,583,674 B2).

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12. As per claims 2-4 and 12-14, Melava et al disclose the invention substantially. Melava et al do not expressly disclose how second circuit is further configured to sequence/present the data signals in response to the second clock signal. However, a routineer in the art would be able to modify the second circuit of the disclosed invention as needed and utilize the second clock signal generated by the disclosed invention accordingly. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second circuit of the disclosed invention by Melava et al as needed. Moreover, the main disclosure of the prescaler architecture would not be affected as to how the second circuit is further configured. In other words, a routineer in the art can configure the circuit as needed without disturbing the main prescaler architecture of the disclosed invention.

13. As per claims 5-6 and 15-16, Melava et al disclose the invention substantially. Melava et al do not disclose how the data are latched presented by the second circuit. However, a routineer in the art would know to use latches to latch data as latches are well known. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a number of latches to latch the data. Moreover, the main disclosure of the prescaler architecture would not be affected as to how the data are latched which are presented by the second circuit.

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14. As per claims 9 and 19, Melava et al disclose the invention substantially. Melava et al do not expressly disclose further dividing the second clock signal to generate a third clock signal and further dividing the third clock signal to generate a fourth clock signal. However, a routineer in the art would be able to do so and Melava et al has shown this with the first clock signal to generate the second clock signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the disclosed circuitry to generate third and fourth clock signals and utilize a gating circuitry to gate the second clock signal received by the second circuit in response to the third and fourth clock signals.

#### ***Allowable Subject Matter***

15. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.



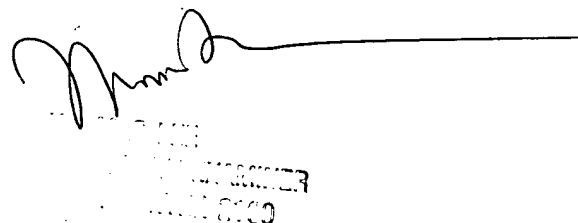
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

December 1, 2004

A handwritten signature in dark ink, followed by a horizontal line. Below the signature is a circular official stamp, partially legible, containing the word "EXAMINER" and the date "DEC 1 2004".